US-PAT-NO: 5953286

DOCUMENT-IDENTIFIER: US 5953286 A

TITLE: Synchronous DRAM having a high data transfer rate

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Detailed Description Text - DETX (13):

The output control clock generating circuit 206 receives the internal clock ICLK and the discrimination values "0" to "m", and generates a clock FCLK having the same clock period (namely, frequency) as that of the internal clock ICLK. Since the internal clock ICLK has the same clock period as that of the clock CLK, the clock FCLK has the same clock period as that of the clock CLK. The output control clock generating circuit 206 can adjust the phase of the output clock OCLK arbitrarily in time. Accordingly, the output control clock generating circuit 206 can cause the output clock OCLK to have completely the same clock period and phase as those of the clock CLK, or alternatively to have a phase in advance to the phase of the clock CLK.

L Number	Hits	Search Text	DB	Time stamp
1	7973	dll (delay adj lock$4 adj loop)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:04
2	119714	phase adj shift$4	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:50
3	146	(dll (delay adj lock$4 adj loop)) near4 (phase adj shift$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:08
4	5406	(phase adj shift$4) near4 "90"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:50
5	13	(dll (delay adj lock$4 adj loop)) same ((phase adj shift$4) near4 "90")	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:58
6	372	(dll (delay adj lock$4 adj loop)) same (phase adj shift$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:58
7	226	((dll (delay adj lock$4 adj loop)) same (phase adj shift$4)) not ((dll (delay adj lock$4 adj loop)) near4 (phase adj shift$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:59
8	3415	transmit adj clock	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 20:59
9	28	(((dll (delay adj lock$4 adj loop)) same (phase adj shift$4)) not ((dll (delay adj lock$4 adj loop)) near4 (phase adj shift$4))) and (transmit adj clock)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 21:17
10	198	(((dll (delay adj lock$4 adj loop)) same (phase adj shift$4)) not ((dll (delay adj lock$4 adj loop)) near4 (phase adj shift$4))) not ((((dll (delay adj lock$4 adj loop)) same (phase adj shift$4)) not ((dll (delay adj lock$4 adj loop)) near4 (phase adj shift$4))) and (transmit adj clock))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 22:34
11	812	arbitra$5 same (phase near2 (adjust$5 correct$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 22:50
12	21284	transmit$4 near3 clock	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 22:43
13	6	(arbitra$5 same (phase near2 (adjust$5 correct$4))) same (transmit$4 near3 clock)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 22:43
14	204	arbitra$5 near6 (phase near2 (adjust$5 correct$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 22:51
15	29	(arbitra$5 near6 (phase near2 (adjust$5 correct$4))) same clock	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/22 22:51